PL602-00

Multiplier XO IC Die for 12 to 25MHz Parallel Resonant Crystals

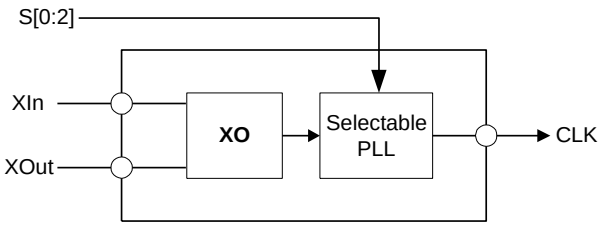
FEATURES

- Integrated crystal oscillator circuitry (XO).
- Low phase noise (-125dBc @ 10kHz offset and 155.52MHz output)
- Selectable frequency multipliers (x1, x2, x4, x8 as bonding options).
- 3.3V supply voltage.
- Uses inexpensive fundamental-mode parallel resonant crystals (from 12 to 25MHz).
- Selectable High Drive (30mA) or Standard Drive (10mA) output.
- Available in DIE (65 mil x 62 mil).

DESCRIPTION

The PL602-00 is a monolithic low jitter and low phase noise (-125dBc @10kHz offset and 155.52MHz output), high performance CMOS XO IC. This flexible device can be used as a XO with output frequencies ranging from F_{XIN} x 1 to F_{XIN} x 8 thanks to selector pads allowing bonding options (see Divider Selection Table on this page). This makes the PL602-00 ideal for a wide range of applications from 12MHz to 200MHz (including 50MHz, 77.76MHz, 125MHz and 155.52MHz, etc.).

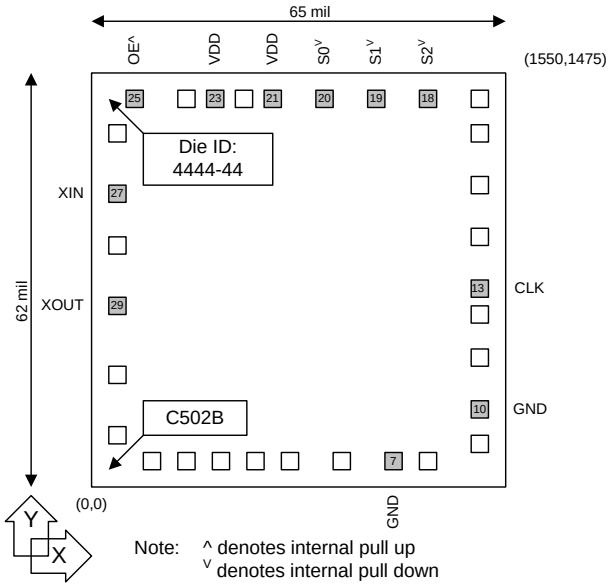
BLOCK DIAGRAM



DIE SPECIFICATIONS

Name	Value
Size	62 x 65 mil
Reverse side	GND
Pad dimensions	80 micron x 80 micron
Thickness	8 mil

DIE CONFIGURATION



MULTIPLIER SELECTION

SELECTION			F_{XIN}	CLK (MHz)
S2	S1	S0		
0	0	0	12MHz – 25MHz	F_{XIN} x 2
0	0	1		F_{XIN} x 4
0	1	0		F_{XIN} x 1
1	0	0		F_{XIN} x 8
0	1	1		F_{XIN} x 2*
1	1	0		F_{XIN} x 4*
1	0	1		F_{XIN} x 1*
1	1	1		F_{XIN} x 8*

Note: - Selector pads default to '0', wire bond to VDD to set to '1'
- (*) High-drive CMOS output

PAD DESCRIPTION

Name	Number	Description
XIN	27	Crystal input connection.
XOUT	29	Crystal connection.
GND	7,10	Ground.
CLK	13	Clock Output.
S[0:2]	18,19,20	Frequency selection pad
VDD	21, 23	3.3V Power Supply.
OE	25	Output Enable: '0' to disable (tri-state output), 1' (default value when not connected) to enabled the output.

ELECTRICAL SPECIFICATIONS

1. Absolute Maximum Ratings

PARAMETERS	SYMBOL	MIN.	MAX.	UNITS
Supply Voltage	V_{DD}		4.6	V
Input Voltage, dc	V_I	-0.5	V_{DD}+0.5	V
Output Voltage, dc	V_O	-0.5	V_{DD}+0.5	V
Storage Temperature	T_S	-65	150	°C
Ambient Operating Temperature*	T_A	-40	85	°C
Junction Temperature	T_J		125	°C
Lead Temperature (soldering, 10s)			260	°C
ESD Protection, Human Body Model			2	kV

Exposure of the device under conditions beyond the limits specified by Maximum Ratings for extended periods may cause permanent damage to the device and affect product reliability. These conditions represent a stress rating only, and functional operations of the device at these or any other conditions above the operational limits noted in this specification is not implied.

* **Note**: Operating Temperature is guaranteed by design for all parts (COMMERCIAL and INDUSTRIAL), but tested for COMMERCIAL grade only.

2. DC Electrical Specifications

PARAMETERS	SYMBOL	CONDITIONS	MIN.	TYP.	MAX.	UNITS
Supply Current, Dynamic, with Loaded Output	I_{DD}	F_{XIN} = 12 - 25MHz Output load of 10pF			35	mA
Operating Voltage	V_{DD}		2.97		3.63	V
Output drive current (High Drive)	I_{OH}	V_{OH}= V_{DD}-0.4V, V_{DD}=3.3V	30			mA
	I_{OL}	V_{OL} = 0.4V, V_{DD} = 3.3V	30			mA
Output drive current (Standard Drive)	I_{OH}	V_{OH}= V_{DD}-0.4V, V_{DD}=3.3V	10			mA
	I_{OL}	V_{OL} = 0.4V, V_{DD} = 3.3V	10			mA

3. AC Electrical Specifications

PARAMETERS	SYMBOL	CONDITIONS	MIN.	TYP.	MAX.	UNITS
Input Crystal Frequency			12		25	MHz
Output Clock Rise/Fall Time (Standard Drive)		0.3V ~ 3.0V with 15 pF load		3.0		ns
Output Clock Rise/Fall Time (High Drive)		0.3V ~ 3.0V with 15 pF load		1.2		
Output Clock Duty Cycle		Measured @ 50% V_{DD}	45	50	55	%

4. Crystal Specifications

PARAMETERS	SYMBOL	CONDITIONS	MIN.	TYP.	MAX.	UNITS
Crystal Resonator Frequency	F_{XIN}	Parallel Fundamental Mode	12		25	MHz
Crystal Loading Rating	$C_{L\ (xtal)}$			20		pF
Recommended ESR	R_E	AT cut			30	Ω

5. Jitter and Phase Noise Specification

PARAMETERS	CONDITIONS	MIN.	TYP.	MAX.	UNITS
RMS Period Jitter (1 sigma – 1000 samples)	at 155MHz, with capacitive decoupling between VDD and GND.		20		ps
Phase Noise relative to carrier Carrier Frequency 44MHz	@100Hz offset		-113		dBc/Hz
	@1kHz offset		-130		dBc/Hz
	@10kHz offset		-135		dBc/Hz
	@100kHz offset		-128		dBc/Hz
	@1MHz offset		-128		dBc/Hz
Phase Noise relative to carrier Carrier Frequency 155.52MHz	@100Hz offset		-100		dBc/Hz
	@1kHz offset		-115		dBc/Hz
	@10kHz offset		-125		dBc/Hz
	@100kHz offset		-116		dBc/Hz
	@1MHz offset		-114		dBc/Hz
	@10MHz offset		-132		dBc/Hz
	@40MHz offset		-142		dBc/Hz

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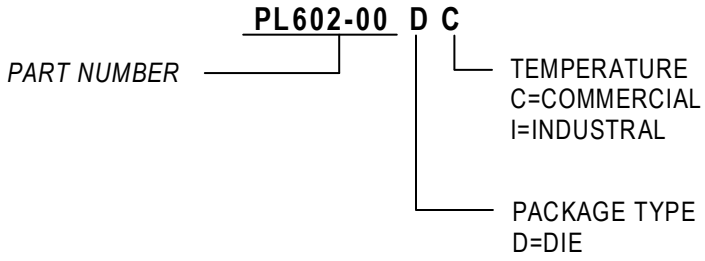
PAD ASSIGNMENT

Pad #	Name	X (μm)	Y (μm)	Description
7	GND	1042	109	Ground.
10	GND	1400	259	Ground.
13	CLK	1400	716	CMOS clock output.
18	S2	1232	1365	Used to select multiplication factor and drive level. Internal pull down.
19	S1	1042	1365	Used to select multiplication factor and drive level. Internal pull down.
20	S0	854	1365	Used to select multiplication factor and drive level. Internal pull down.
21	VDD	659	1365	3.3V power supply.
23	VDD	459	1365	3.3V power supply.
25	OE	194	1365	Used to enable/disable the output(s). Internal pull up.
27	XIN	109	1017	Crystal input. See crystal specification page 3.
29	XOUT	109	646	Crystal output. See crystal specification page 3.

ORDERING INFORMATION

For part ordering, please contact our Sales Department:
2180 Fortune Drive, San Jose, CA 95131, USA
Tel: (408) 944-0800 Fax: (408) 474-1000

PART NUMBER
The order number for this device is a combination of the following:
Device number, Package type and Operating temperature range



Order Number	Marking	Package Option
PL602-00DC	P602-00DC	Die – Waffle Pack

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